CHIMEI INNOLUX DISPLAY CORPORATION

LCD MODULE

APPLICATION NOTE

Customer:	**All**
LCD SIZE:	**10.2D1**
Date:	**2010/03/01**
Version:	**I**

Remark
■ **With PCB**

Approved by	Reviewed by	Prepared by
Hans Chen 2010/03/02	**Peter Wang** 2010/03/02	**Sandan.Deng** 2010/03/01

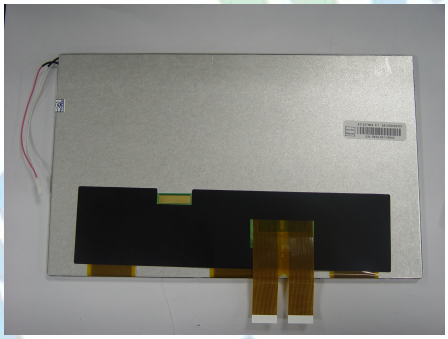
Chimei Innolux Display Corporation
Industry District 10, LongHua, Shen, Ch
T.L +86-0755-27706888

Record of Revision

Version	Revise Date	Page	Content
A	2008/05/15		New version and standardization
B	2008/08/06		Add new LCM AT102TN42
C	2008/09/25		Add new LCM AT102TN03 V.3
D	2009/03/03		Modify format
E	2009/05/13	11	Modify Gamma Reference Circuit
F	2009/06/30	13	Modify the power IC vendor
G	2009/07/30	9	Add timing diagram
H	2009/09/01		Modify DC-DC Reference Circuit and add BOM List
I	2010/03/01		Modify VGH voltage

1. Module Introduction

1.1 Module Photo

Model name	Top	Bottom
AT102TN03 V.8 AT102TN03 V.9 AT102TN03 V.A		

1.2 Module Comparison Table

Model name	Interface	Brightness(nits)	TSP	Connector
AT102TN03 V.8	TTL	350	Without	AF 730L-A2G1T
AT102TN03 V.9	TTL	250	Without	AF 730L-A2G1T
AT102TN03 V.A	TTL	280	With	AF 730L-A2G1T

2. Pin Assignment Table

Pin No.	Symbol	I/O	Function	Remark
1	POL	I	Polarity selection	
2	STVD	I/O	Vertical start pulse input when U/D= H	
3	OEV	I	Output enable	
4	CKV	I	Vertical clock	
5	STVU	I/O	Vertical start pulse input when U/D= L	
6	GND	P	Power ground	
7	EDGSL	I	Select rising edge or rising/falling edge	

8	V_{CC}	P	Power supply for digital circuit	
9	V9	I	Gamma voltage level 9	
10	V_{GL}	P	Gate OFF voltage	
11	V2	I	Gamma voltage level 2	
12	V_{GH}	P	Gate ON voltage	
13	V6	I	Gamma voltage level 6	
14	U/D	I	Up/down selection	
15	V_{COM}	I	Common voltage	
16	GND	P	Power ground	
17	AV_{DD}	P	Power supply for analog circuit	
18	V14	I	Gamma voltage level 14	
19	V11	I	Gamma voltage level 11	
20	V8	I	Gamma voltage level 8	
21	V5	I	Gamma voltage level 5	
22	V3	I	Gamma voltage level 3	
23	GND	P	Power ground	
24	R5	I	Red data(MSB)	
25	R4	I	Red data	
26	R3	I	Red data	
27	R2	I	Red data	
28	R1	I	Red data	
29	R0	I	Red data(LSB)	
30	GND	P	Power ground	

31	GND	P	Power ground	
32	G5	I	Green data(MSB)	
33	G4	I	Green data	
34	G3	I	Green data	
35	G2	I	Green data	
36	G1	I	Green data	
37	G0	I	Green data(LSB)	
38	STHL	I/O	Horizontal start pulse input when R/L = L	
39	REV	P	Control signal are inverted or not	
40	GND	I	Power ground	
41	DCLK	I	Sample clock	
42	DV_{DD}	P	Voltage for digital circuit	
43	STHR	I/O	Horizontal start pulse input when R/L = H	
44	LD	I	Latches the polarity of outputs and switches the new data to outputs	
45	B5	I	Blue data (MSB)	
46	B4	I	Blue data	
47	B3	I	Blue data	
48	B2	I	Blue data	
49	B1	I	Blue data	
50	B0	I	Blue data (LSB)	
51	R/L	I	Right/ left selection	
52	V1	I	Gamma voltage level 1	
53	V4	I	Gamma voltage level 4	

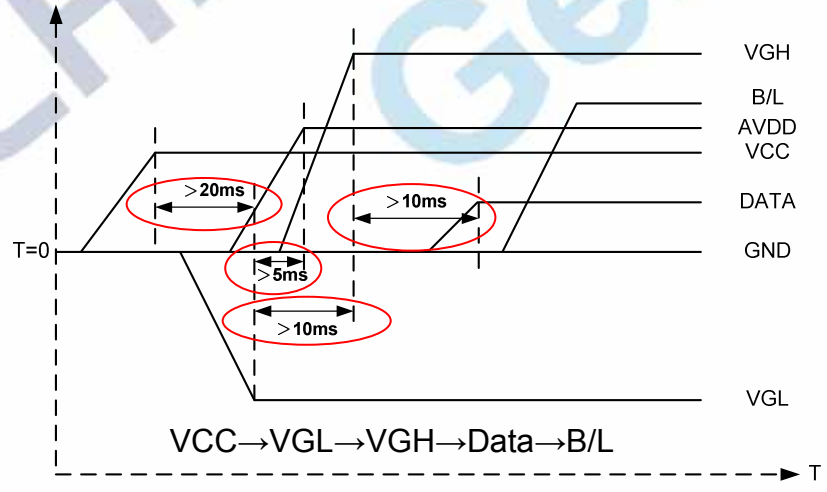
54	V7	I	Gamma voltage level 7	
55	V10	I	Gamma voltage level 10	
56	V12	I	Gamma voltage level 12	
57	V13	I	Gamma voltage level 13	
58	AV_{DD}	P	Voltage for analog circuit	
59	GND	P	Power ground	
60	V_{COM}	I	Common voltage	

3. Power &Timing Characteristic

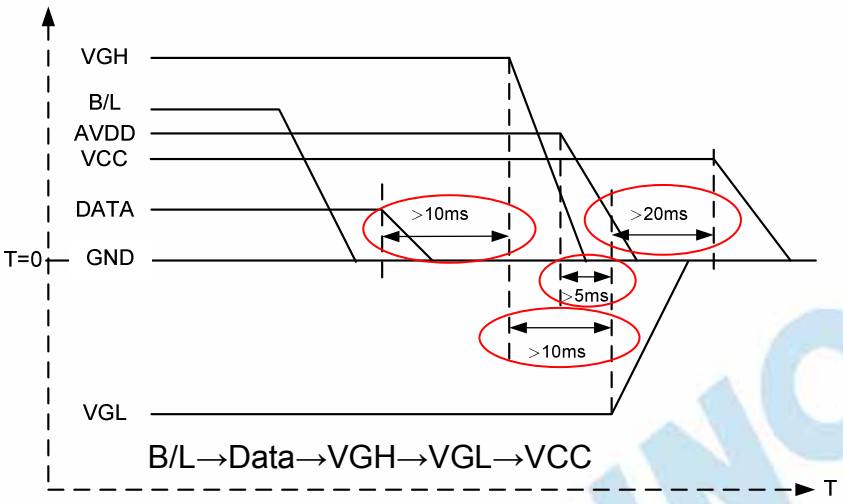
3.1. Power Sequence

Customer should follow our product power sequence, other it would lead to display abnormal, please refer to the figures as below.

Power on:



Power Off :



Note: Data includes POL, STVD, OEV, CKV, STVU, EDGSL, STHL, REV, DCLK, V_{CC}, STHR, LD.

3.2 Power Operation Conditions

Customer should notice the red mark specially, if you do not follow it, it would lead to display abnormal.

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	V_{CC}	3.0	3.3	3.6	V	Note 2
	AV_{DD}	9.0	9.2	9.4	V	
	V_{GH}	15.3	16	16.7	V	
	V_{GL}	-7.7	-7	-6.3	V	
Input signal voltage	V_{COM}	3.65	3.85	4.05	V	
	V1~V7	0.4 A_{VDD}	-	A_{VDD} -0.1	V	
	V8~V14	0.1	-	0.6 A_{VDD}	V	
Input logic high voltage	V_{IH}	0.7V_{CC}	-	V_{CC}	V	Note 3
Input logic low voltage	V_{IL}	0	-	0.3V_{CC}	V	

Note 1: Be sure to apply V_{CC} and V_{GL} to the LCD first, and then apply V_{GH}.
Note 2: V_{CC} setting should match the signals output voltage (refer to Note 3) of customer's system board.
Note 3: STHL, STHR, OEH, L/R, CPH1~CPH3, STVD, STVU, OEV, CKV, U/D.

3.3 Timing Description

Input signals must follow our timing specification, Otherwise the LCM will display abnormally.
About the detail timing parameters of LCD display, please follow the product specification.

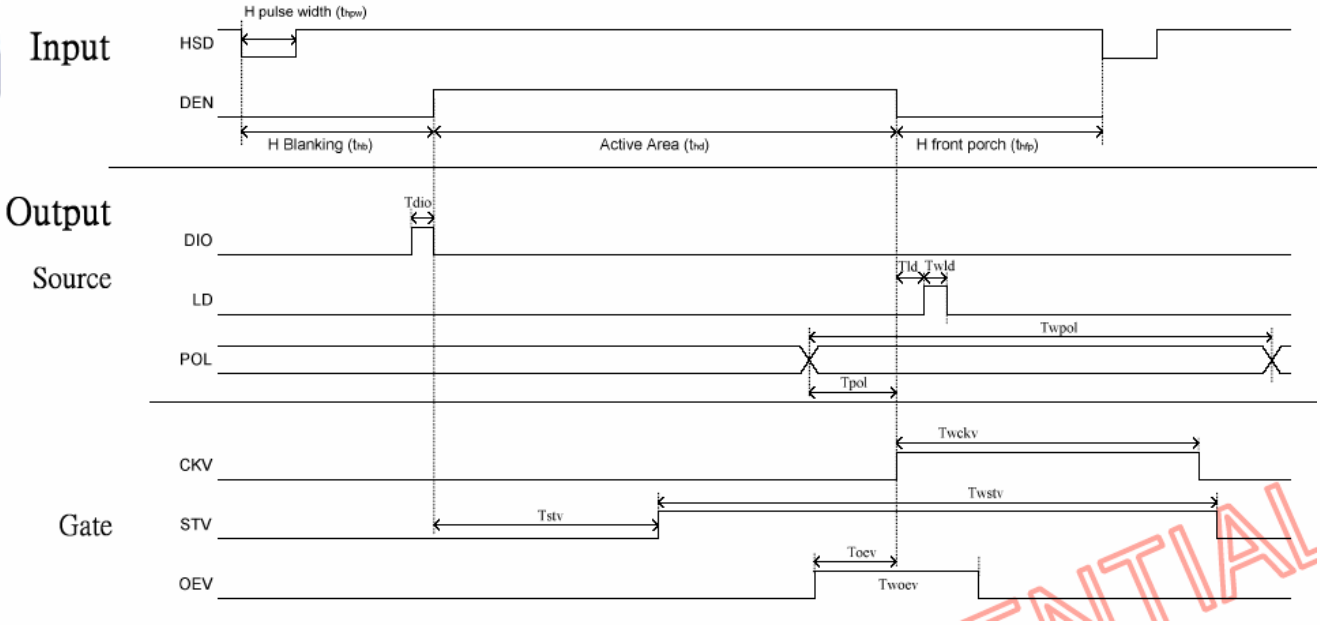
Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DCLK frequency	F_{dclk}	-	40	45	MHz	
DCLK cycle	T_{cph}	22	25	-	ns	
DCLK pulse width	T_{cw}	8	-	-	ns	
Data set-up time	T_{su}	4	-	-	ns	
Data hold time	T_{hd}	2	-	-	ns	
Time that the last data to LD	T_{ld}	1	-	-	Tcph	
Pulse width of LD	T_{wld}	2	-	-	Tcph	
Time that LD to STHL/R	T_{lds}	5	-	-	Tcph	
POL set-up time	T_{psu}	6	-	-	ns	
POL hold time	T_{phd}	6	-	-	ns	
CKV frequency	F_{vclk}	-	-	200	KHz	
CKV rise time	T_{rck}	-	-	100	ns	
CKV falling time	T_{fck}	-	-	100	ns	
CKV pulse width	P_{WCLK}	500	-	-	ns	
Horizontal display timing range	T_{dh}	-	800	-	Tcph	
Horizontal timing range	T_h	-	1056	-	Tcph	
STVU/D setup time	T_{suv}	200	-	-	ns	
STVU/D hold time	T_{hdv}	300	-	-	ns	
STVU/D delay time	T_{dt}	-	-	500	ns	
Driver output delay time	T_{do}	-	-	900	ns	
Output rise time	T_{tlh}	-	500	1000	ns	

Output falling time	T_{thl}	-	400	800	ns	
OEV pulse width	T_{wcl}	1	-	-	us	
OEV to Driver output delay time	T_{oe}	-	-	900	ns	
Horizontal lines per field	T_v	512	525	610	Line	
Vertical display timing range	T_{vd}	-	480	-	Line	

3.4 Timing Diagram

3.4.1 Input & output timing

Parameter	Symbol	Value	Unit
Source			
Dio rising to first data	Tdio	1	DCLK
Last data to LD rising	Tld	12	DCLK
LD pulse width	Twld	4	DCLK
POL transition to last data	Tpol	1/16	H
POL cycle time	Twpol	1	H
Gate			
CKV pulse width	Twckv	0.5	H
First data to STV rising	Tstv	0.5	thd
STV pulse width	Twstv	1	H
OEV to last data	Toev	1/16	H
OEV pulse width	Twoev	1/8	H

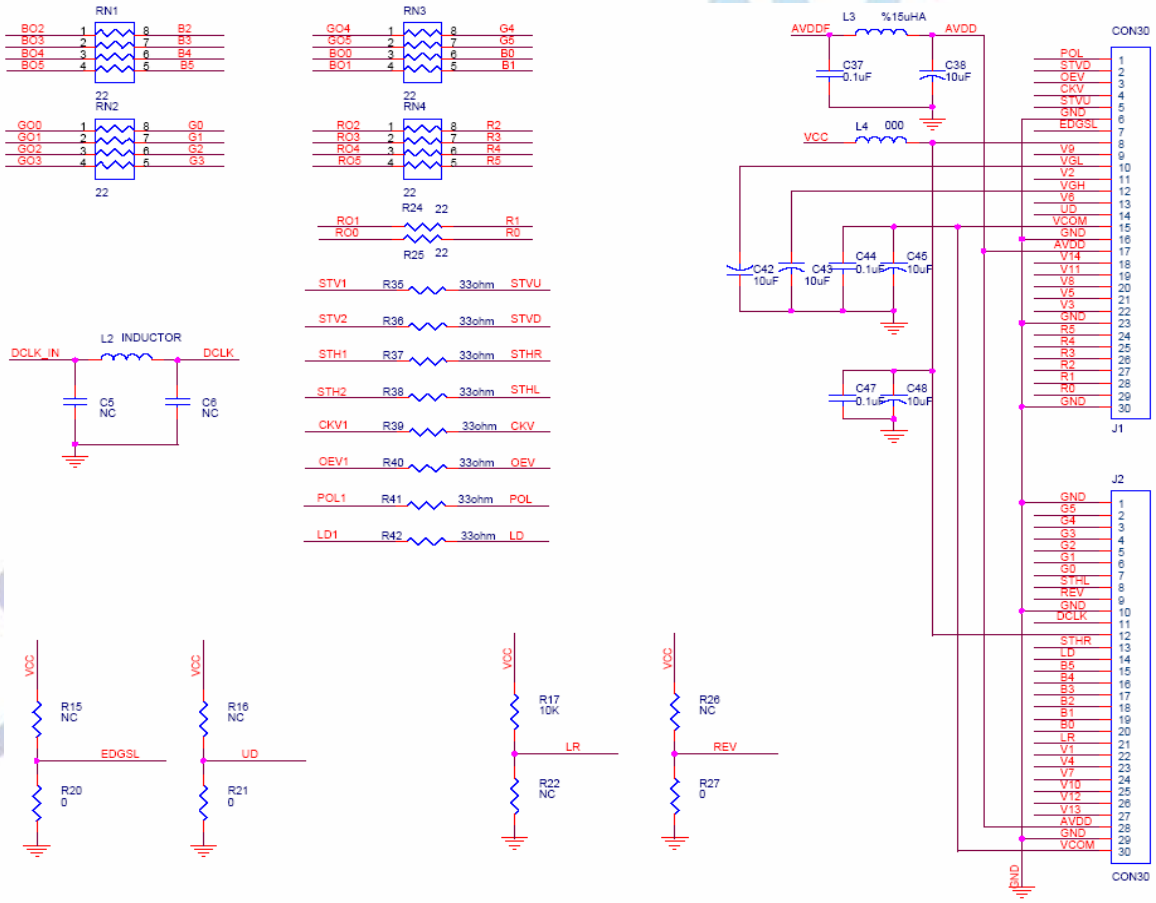


4. Software Introduction

NA

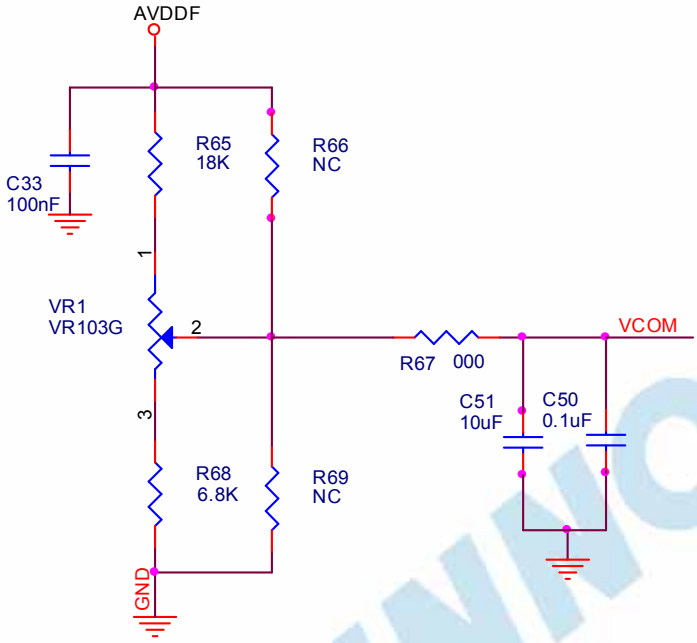
5. Reference Circuit

5.1 Interface reference circuit

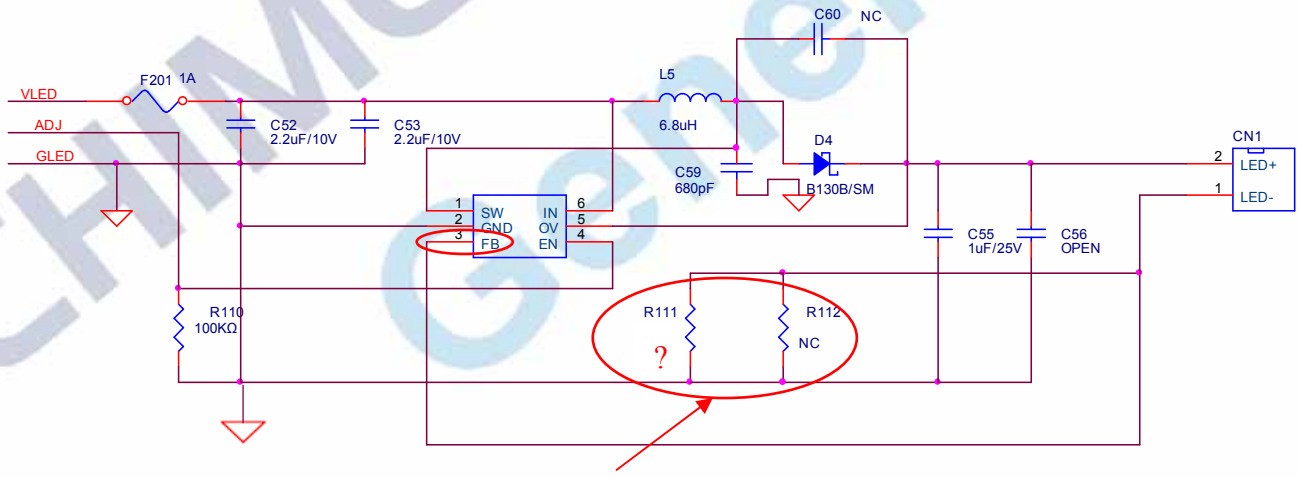


5.2 Vcom Reference Circuit

We suggest our customer using the below circuit to design the Vcom voltage. The Vcom voltage adjustment range is 3.6V ~ 4.0V.

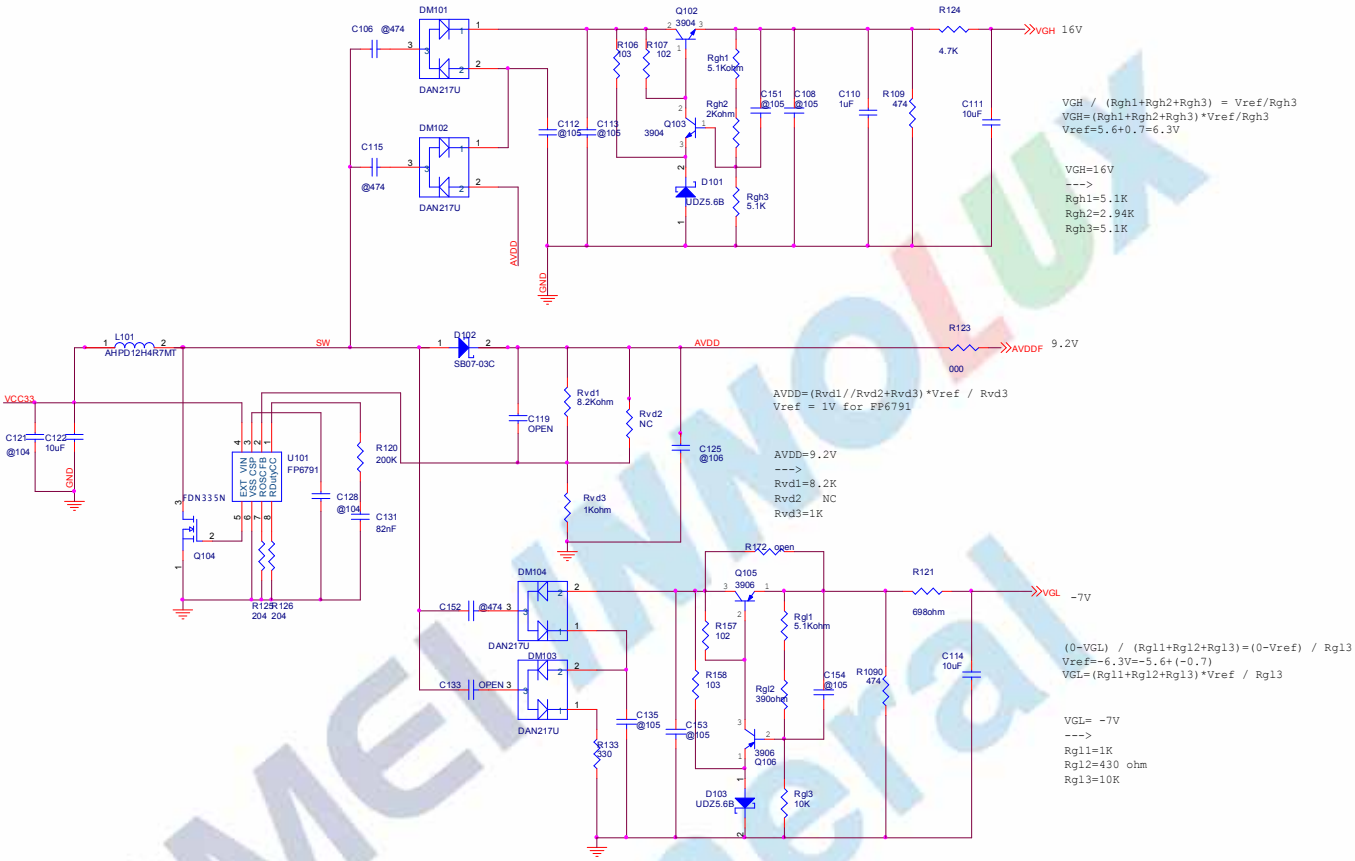


5.3 Backlight Driver Reference Circuit



Note: I = V_{FB} / (R111 // R112)

5.4 DC/DC Reference Circuit & BOM list



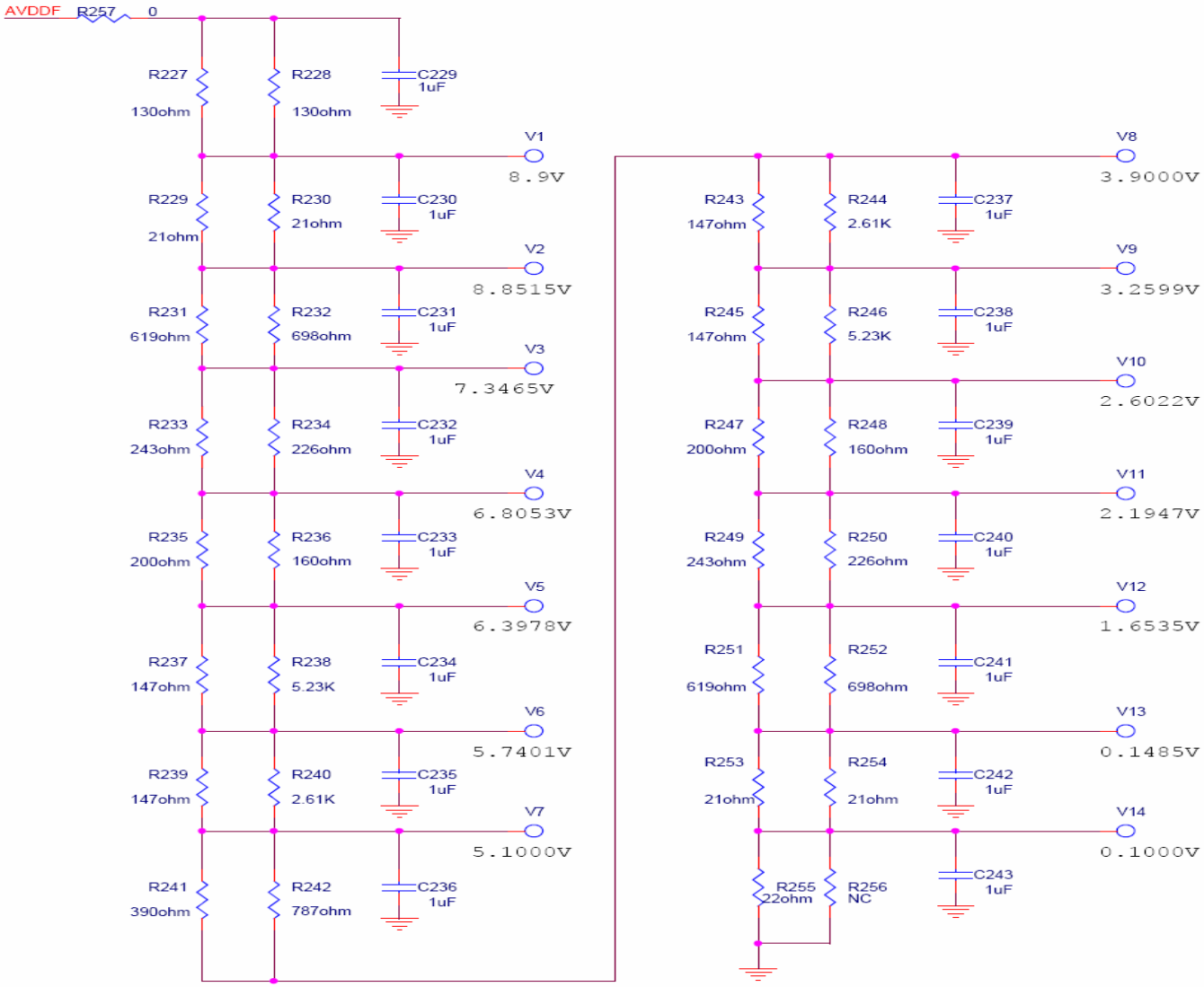
BOM List			
Item	**Quantity**	**Reference**	**Description**
1	1	U101	PWM IC FP6791,8 PIN TSSOP, Fitipower
2	4	DM101,DM102,DM103,DM104	Diode module DAN217U, Rohm
3	2	Q102,Q103	TRANSISTOR(NPN) ,MMST3904,SC-59,Rohm
4	2	Q105,Q106	TRANSISTOR(PNP) ,MMST3906,SC-59,ROHM
5	1	Q104	MOSFET N-channel,FDN335N,SOT-23,Fairchild
6	2	D101,D103	Zener Diode,UDZ5.6B,SOD-323.Rohm
7	1	D102	SCHOTTKY BARRIER DIODE.SB07-03C, Sanyo

5.5 Gamma Reference Circuit

When you use InnoLux 10.2D1 digital LCD, you must use the below gamma voltage circuit to design your system. And it is the most important to set the gamma voltage value according to the gamma voltage table. If you don't do it, the product will not be displayed normally.

The theory voltage while loading 10.2D1 LCD (V)	The theory resistance(Ω)	The actual resister on control board(Ω)
AVDD=9.2	65	R57=130 // R58=130
V1=8.9	10.5	R64=21 // R65=21
V2=8.8515	328.1	R69=619 // R70=698
V3=7.3465	117.1	R74=243 // R75=226
V4=6.8053	88.9	R77=200 // R78=160
V5=6.3978	143	R82=147 // R83=5230
V6=5.7401	139.2	R88=147 // R89=2610
V7=5.1	260.8	R93=390 // R94=787
V8=3.9	139.2	R98=147 // R99=2610
V9=3.2599	143	R102=147 // R103=5230
V10=2.6022	88.9	R106=200 // R107=160
V11=2.1947	117.1	R109=243 // R110=226
V12=1.6535	328.1	R111=619 // R112=698
V13=0.1485	10.5	R114=21 // R115=21
V14=0.1	22	R116=22 // R117(open)
Remark : 1. Please set the AVDD voltage at 9.2V(optimum) accurately, and the maximum tolerance is ±0.2V.		

Gamma Table for 10.2D1 LCD



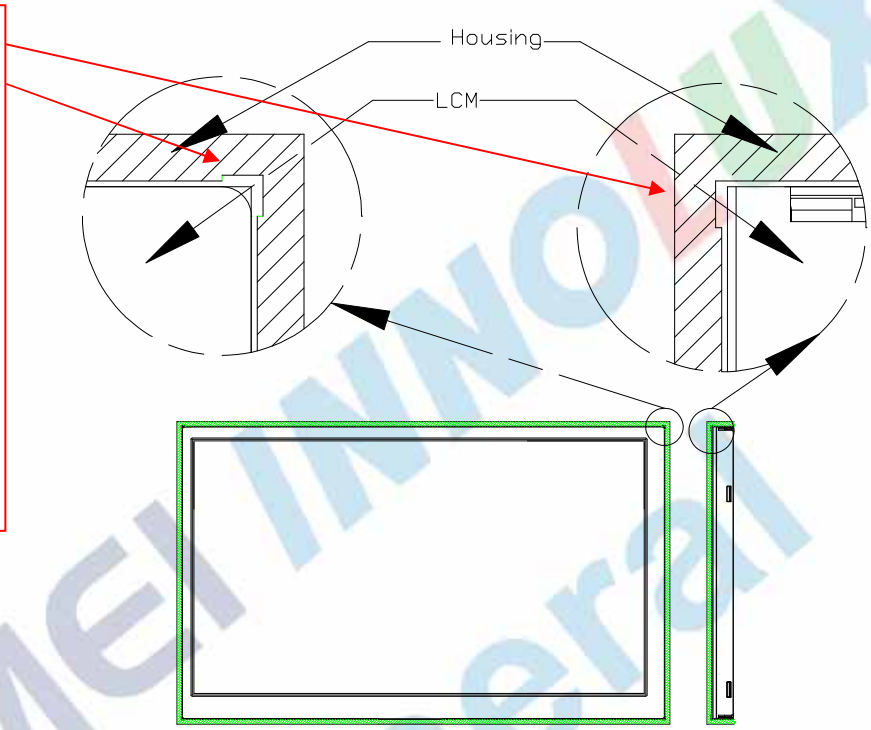
5.6 Vendor Recommend

Item	Vendor	Type	Remark
DC/DC	Fiti Power	FP6791	
LED Driver	Fiti Power	FP6745	PWM Frequency:100Hz~50KHz

6. Suggestions for housing design.

6.1 LCM corner /edge avoidable cutting.

If you design a avoidable cutting as the right drawing. LCM will easier to assemble in the housing.
When you use the LCM with TSP, the cutting will avoid damage the edge or corner of TSP during the assembly.

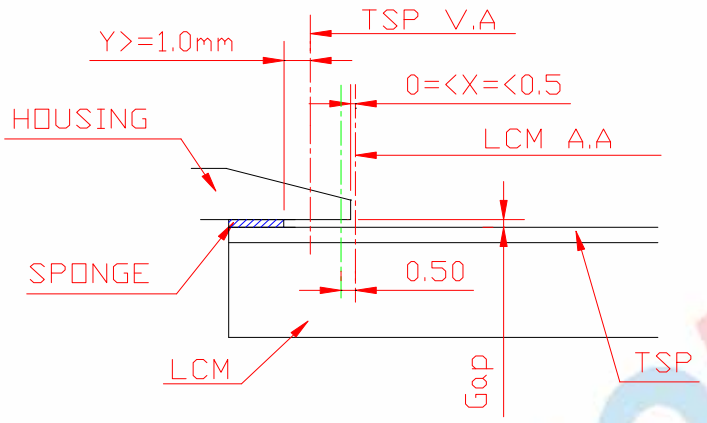


Suggestions of housing design

6.2 Housing opening design guide.

6.2.1 With TSP

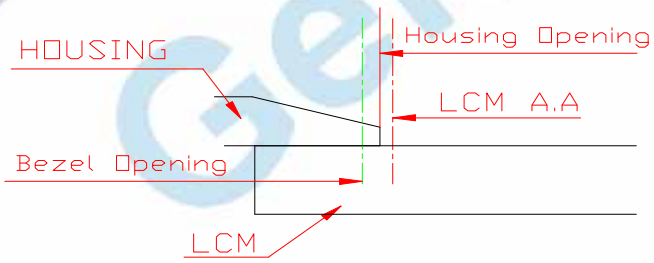
Because touch film is made of flexible PET, any unexpected touch with it would cause malfunction of touch panel. So here a sponge between touch panel and plastic housing is recommended for users. And the drawing will show you how to design the housing and sponge.



Section sketch (with TSP)

Notes: 1. X is the distance from LCM A.A to housing opening.
2. Y is the distance from TSP V.A to Sponge opening.
3. The active force will be bigger when you touch the area near the housing opening.
4. If you want to provide more protection for LCM, you can add same buffer material on the bottom of LCM.

6.2.2 Without TSP

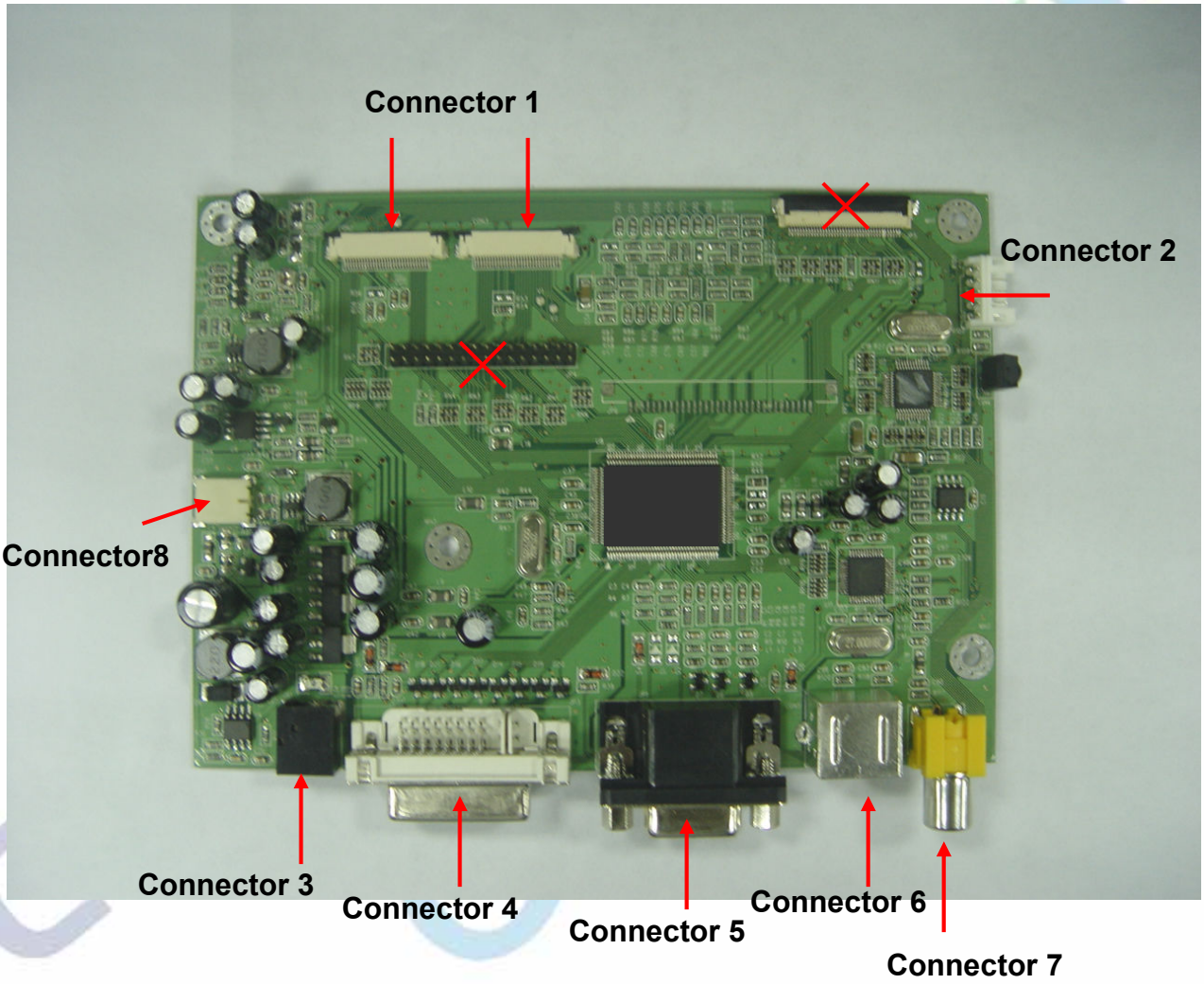


Section sketch(without TSP)

Notes: 1. Housing opening mast bigger than LCMA.A and cover the bezel .
2. If you want to provide more protection for LCM, you can add same buffer material on the top or bottom of LCM.

7. Demo Board Introduction

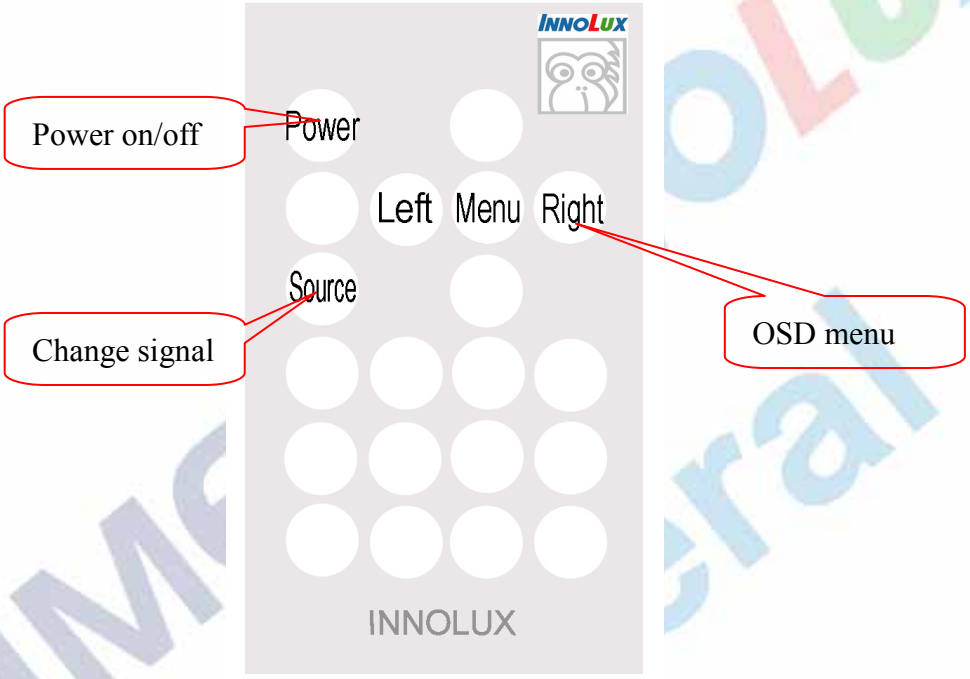
7.1 Interface of demo board



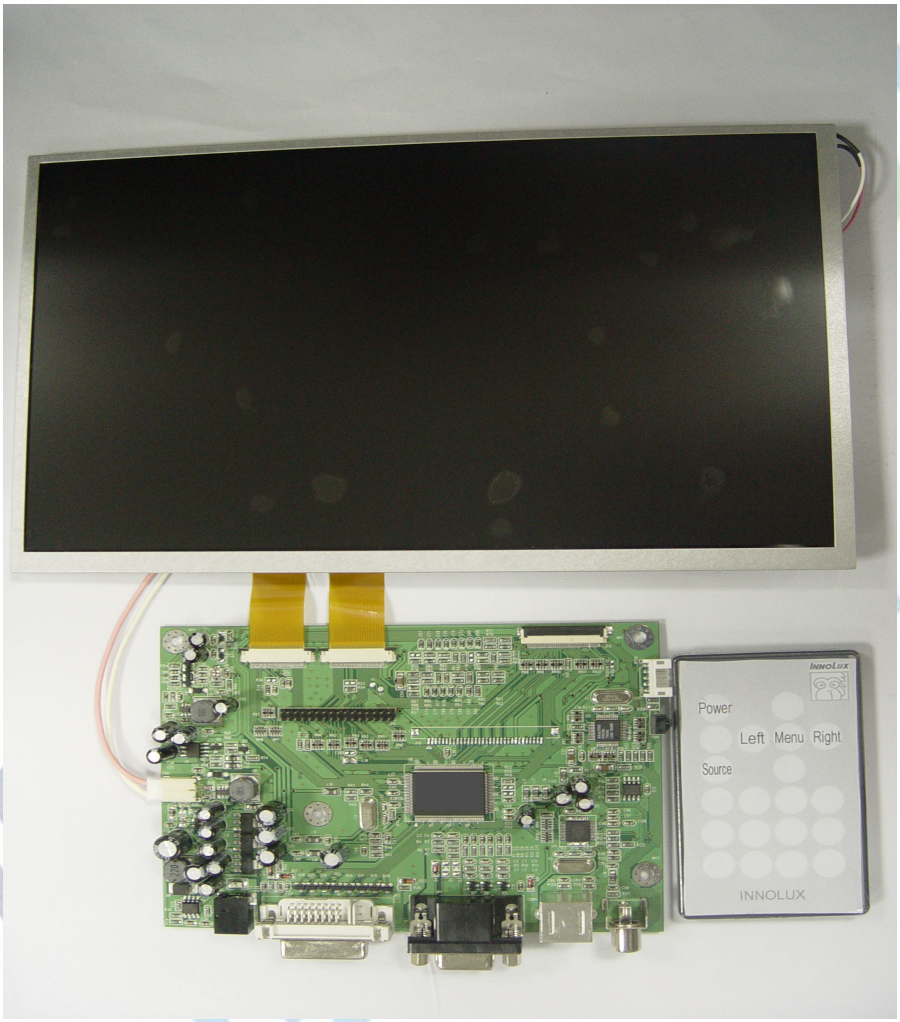
Connector	I/O	Function
1	O	10.2D1 FPC connector
2	I	The hand-off controller of CVBS and D-Sub
3	P	12V DC input
4	I	DVI signal input
5	I	VGA signal input

6	I	S-video
7	I	CVBS
8	O	LED connector

7.2 Interface of Remote Control



7.3 Linking LCM

AT102TN03


Notes:

1. We don’t guarantee any power & timing & optical characteristic measure by INL control board.
2. INL control board is just for demo INL digital panel.